PROGRESS REPORT
07/11/03

To: Martha Symko-Davies, Technical Contract Monitor, NREL

From: D. L. Morel and C. S. Ferekides/University of South Florida

CC: ***Carolyn Lopez, NREL, Anne Gallacher/USF DSR***

Re: Quarterly Report for subcontract **NAT-1-30620-08** for the period 11/09/02 – 2/08/03

CdSe

Record Jsc's

Recently we deposited CdSe on NREL supplied tin oxide as part of a collaborative effort with David Young to evaluate alternative p contacts. We added our standard ZnSe/Cu contact to one of the substrates for evaluative purposes and measured a surprisingly high Jsc. The QE plot for three devices from the substrate is shown at right along with a table of the Jsc breakdown. As can be seen three devices exhibit a Jsc in excess of 17 mA/cm^2. This is believed to be a record for a thin-film solid state CdSe device, especially one that is transparent. The Jsc for device 1 of 17.4 mA/cm^2 is 2.7 mA/cm^2 higher than our previous best 14.7 and is rapidly approaching the previously highest reported *internal* Jsc of 18.3. *With this level of Jsc we have now attained one of the three parameters needed to produce transparent CdSe devices in the 15 – 16% range that are needed to reach our tandem objective of 25%.* This also confirms our earlier assertion

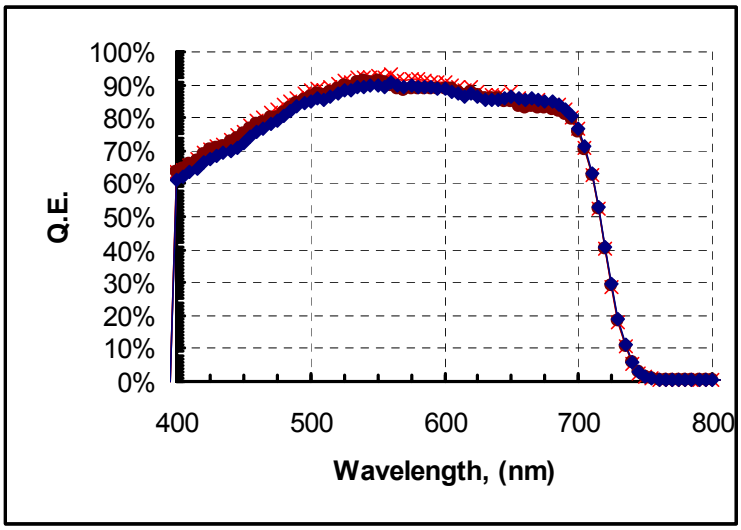

Figure 1. QE spectra of three TO/CdSe/ZnSe/Cu devices with Jsc in excess of 17 mA/cm^2 .

			Current from devic #1	Current from devic #2	Current from devic #3
	From (nm)	To (nm)	Jsc		
Region #1	300	400	0.103792	0.104169	0.099717
Region #2	400	510	4.591033	4.523851	4.415128
Region #3	510	650	8.763002	8.58872	8.562275
Region #4	650	800	3.948719	3.892821	3.978698
Region #5	800	900	0.019022	0.019676	0.023016
Total Jsc=			17.42557	17.12924	17.07883

Table 1. Jsc breakdown for the devices of figure 1.

that we are producing high electronic quality CdSe. If we can develop the contacts to produce Voc's in the range of 1 volt, we will achieve our objective.

As discussed previously the ZnSe/Cu contact is complex and not well understood. However, the TO/CdSe/ZnSe/Cu structure has proved to be a reliable format for evaluating the electronic properties of CdSe. Since the ZnSe/Cu contact is nominally the same from run to run we have to conclude that the increased Jsc is due to the NREL TO. Additional experiments have been planned to follow-up on this result. At this point we can only speculate that the TO has had a favorable impact on the microstructure of the CdSe.

Back Contact Issues

In our last report we reported improvement in Voc by use of ZnTe front contacts. We also presented results of initial modeling efforts to match operation of our current devices. These efforts focused on ZnTe/CdSe because of the improved Voc's. The band diagram for the current model is shown again for convenience in figure 2. Several issues regarding the model and the implication of those issues to device performance were raised, and we wish to follow-up on those here. The most important issue is the location of the contacts. As seen in figure 2, the front contact is close to the ZnTe valence band, while the back contact is near mid-gap. If this is true, then further improvement in Voc would rest largely on lowering the back contact energy. In figure 3 are shown the relative band profiles for candidate contacts to CdSe. The energy scale is that used by the NREL theory group[1], and the dashed lined is the p-type "pinning energy". What we are concerned with here, however, is the n-type, or back contact.

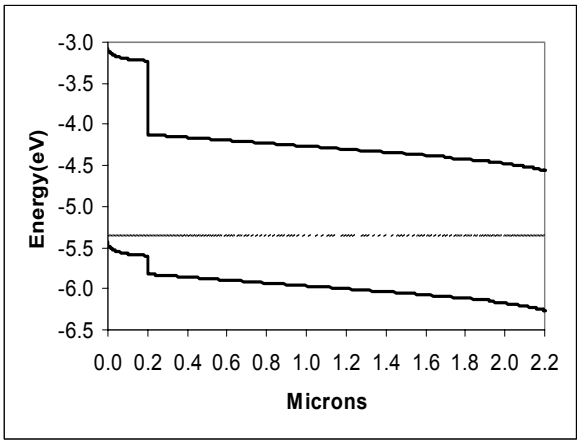

Figure 2. AMPS generated band diagram for ZnTe/CdSe device.

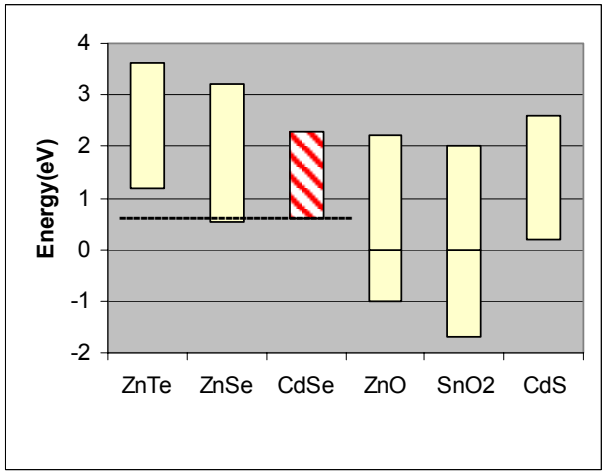

Figure 3. Relative band profiles for contacts to CdSe.

As can be seen, the bottom of the conduction band for SnO_2(TO) is about 0.3 eV below that of CdSe, and since TO is degenerate, its contact energy should be no more than about 0.25 eV from the conduction band of CdSe. Nevertheless, as seen in figure 2, the effective contact energy of the back contact used in the model is about 0.8 eV below the CdSe conduction band. If

this is true, it suggests that the growth of CdSe on TO produces interface states that result in an effective contact energy much lower than the stand-alone energies indicated in figure 3. Actually the energy for SnO_2 in figure 3 is from a separate reference and hence has more uncertainty than the II-VI compounds. This leaves some room for error in the expected band alignments. However, ZnO and CdS are from the same data set, and thus their stand-alone offsets are more reliable. As such it is likely that both have lower contact energy than TO and should result in an improved contact and higher Voc.

We have completed several runs of CdSe on ZnO, and the performance is generally inferior to TO devices. Voc is lower, rather than higher, and all devices exhibit a high series resistance. The latter effect is partially attributable to lowering of the ZnO conductivity during CdSe deposition at temperatures above 400 EC. The ZnO that we have used to date is deposited at about 100 EC. We have measured the change in conductivity at CdSe deposition temperatures, and while there is a decrease, it is not large enough to explain the magnitude of the series resistance that is observed. It is apparent that there is interaction between the CdSe and ZnO during CdSe deposition. Whatever is formed results in a larger effective contact energy that lowers Voc. In addition, a highly resistive layer is formed that results in a high series resistance. To pursue this further we will try depositing ZnO at higher temperatures. This may at least densify the film and make it less susceptible to attack during CdSe deposition.

Although our efforts with ZnO back contacts have not yet proved fruitful, some success is being realized with CdS. As we know, CdS has served as a reliable component in many thin-film solar cell structures. Nevertheless, its role is not easily understood, and that might be expected here. On the one hand one could argue that since CdTe works so well on CdS/TO, CdSe should work as well. On the other hand, CdSe is more prone to be n-type, and according to the band alignments of figure 3 CdS at the rear should produce a barrier to electron collection. This is not the case for CdTe since its conduction band lines up nicely with that of CdS. As seen in figure 3, the unfavorable conduction band offset between CdS and CdSe is about 0.3 eV. This is normally enough to cause problems, and preliminary simulations using the classical physics models of AMPS indicates that this is the case. Nevertheless, the ZnSe/CdSe/CdS/TO devices that we have made to date are exhibiting interesting behavior. In figure 4 we show a comparison of IV curves with a typical ZnSe/CdSe/TO baseline device. These devices typically have Voc's in the 250 – 300 mV range. The encouraging part of this result is that there is about a 50 mV increase in Voc for the CdS devices. This is in keeping with the expectation of lower contact energy, but it is not conclusive evidence that such is the case. First of all, because of the

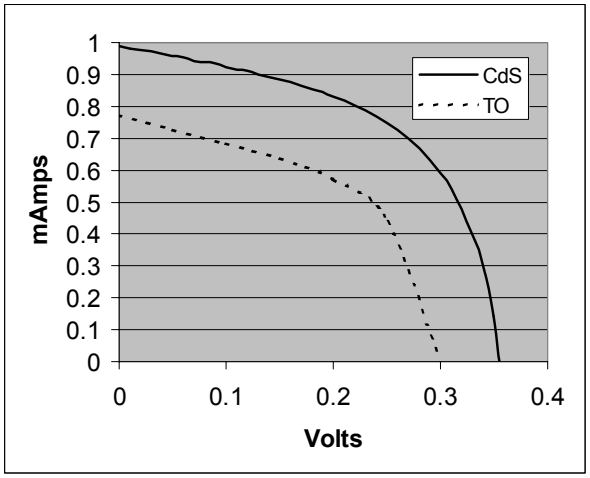

Figure 4. IV curves for a baseline ZnSe/CdSe/TO device and a ZnSe/CdSe/CdS/TO device.

barrier imposed by the stand alone conduction band offset the performance of these devices is not following convention. The fact that the power curve is reasonable indicates that somehow electrons are successfully moving through the CdSe/CdS interface. Two possibilities arise. One is that again the intermingling of CdS and CdSe results in more favorable band offset than expected from figure 3. Another is that the band offset is there, but there is some type of non-conventional electron transport through this region. In either case however, a lower effective contact energy results that produces an increase in Voc. This supports the model of figure 2 indicating that there is room for additional upward movement of the back contact. While this is an encouraging result, it raises a number of additional issues that must be sorted out if we are going to capitalize on these bits of incremental progress. For example, one might also argue that the Voc increase is due to passivation of the CdSe/TO interface and not to improved contact energies. We have preliminary simulation results that indicate that this could be the case, but neither our experimental results or simulations are conclusive at this point. More probing is needed.

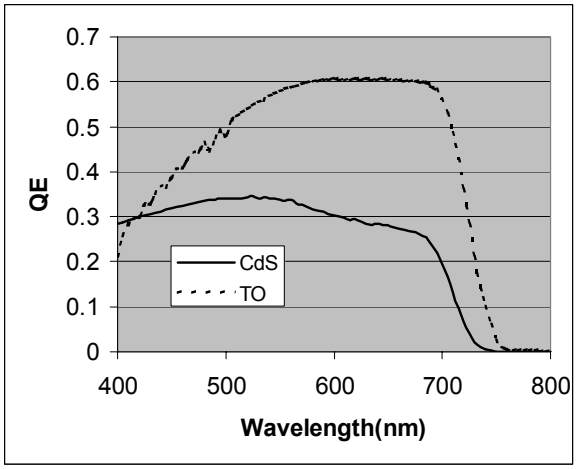

Figure 5. QE plots for ZnSe/CdSe/TO and ZnSe/CdSe/CdS/TO devices.

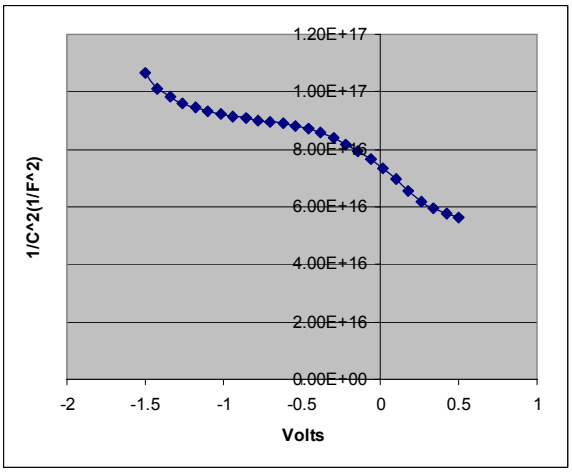

Figure 6. Typical $1/C^2$ vs. V plot for a ZnSe/CdSe device.

Although the current is also higher for the CdS device, this is misleading. A correct comparison of the current density results from the QE plots is provided in figure 5. As can be seen, Jsc for the CdS device is about half of that of the baseline device on TO. This is another observation that is not straightforward to understand. The differences in Isc from the IV curves are often due to differences in device area. However in this case the correction for area is not more than a factor of two as suggested by the IV and QE plots. It seems that under the low light conditions used for QE plots current is suppressed for the CdS devices. This may be due to the CdS layer itself since light is incident from the other side unlike the situation for CdS/CIGS and CdS/CdTe devices.

To improve our understanding of the mechanisms occurring at the back contact it is appropriate to shine light from the backside. According to the model of figure 2 the

CdSe is nearly depleted, and hence the electric field is strong throughout the absorber layer. In figure 6 we show an experimental $1/C^2$ vs. V plot for a ZnSe/CdSe device. As can be seen, the behavior is reasonably flat and does not extrapolate to a reasonable Vbi. This is indicative of depletion and is the basis for choosing this condition in our model. In principle then, if the transport properties for holes and electrons were the same, shining light from the rear should produce the same response as from the front. In practice what we see is a very feeble response for rear light incidence. Photocurrents are down by more than an order of magnitude, and Voc's are only about 100 mV. This suggest that transport for holes is much inferior to that for electrons. We have stated on a regular basis that fermi level location is not important, and it is not under depletion conditions. However, transport properties are important if we wish to have light incidence from either side. CdSe is normally n-type. This is more a statement of transport properties than of fermi level location. That is, it is apparently the case that in our films electron transport is superior to that of holes even if the fermi level is near mid gap or somewhat below as depicted in our model. The implication of these results is that we will have to shine light from the p contact side to get maximum output. However, these devices are 2 μm thick. As we decrease their thickness to the desired level of 0.6 – 0.8 μm, we will see some improvement in backside illumination performance. But based upon the small signals we are seeing at 2 μm thickness we do not expect to achieve parity with front side performance at any reasonable thickness. This is not a major shortcoming, just a limitation in our options.

$Cd_{1-x}Zn_xTe$

Work on CZT-based thin film solar cells has continued. The primary limitation in the performance of these devices appears to be the electronic properties of the absorber itself. A key feature of CZT solar cells is a strong wavelength dependence of their spectral response, which decreases with wavelength indicating that collection in these films is very inefficient.

Processing Issues

In a previous report it was mentioned that CZT films prepared by the co-close-spaced sublimation process were found to contain pinholes and it was suggested that this behavior was to a certain extent related to the type of substrate used (i.e. window layer). Figure 7 shows SEM images of CZT films deposited on CdS (top) and SnO_2 (bottom). Although the grains of the CZT film deposited on CdS appear to be well developed, they do not appear to form a continuous and dense layer; this particular film is an "extreme" case, and was used to demonstrate the structural differences originating from the use of various window layers. On the other hand the CZT film deposited on SnO_2 appears dense, although the grain size variation appears to be large (from about 1 to 3+ μm). It is interesting to note that this behavior is exactly the opposite of that has been previously observed with CdTe films prepared by the CSS process. Such films are dense and continuous when deposited on CdS but can contain pinholes when deposited on SnO_2. In order to continue solar cell fabrication, the pinhole problem has been addressed by using ZnTe as a back contact (also deposited by CSS). The use of ZnTe as a back contact (thickness of approximately 2 μm) appears to "plug" the pinholes and eliminate shorts in the devices. However, it should also be noted that these results also

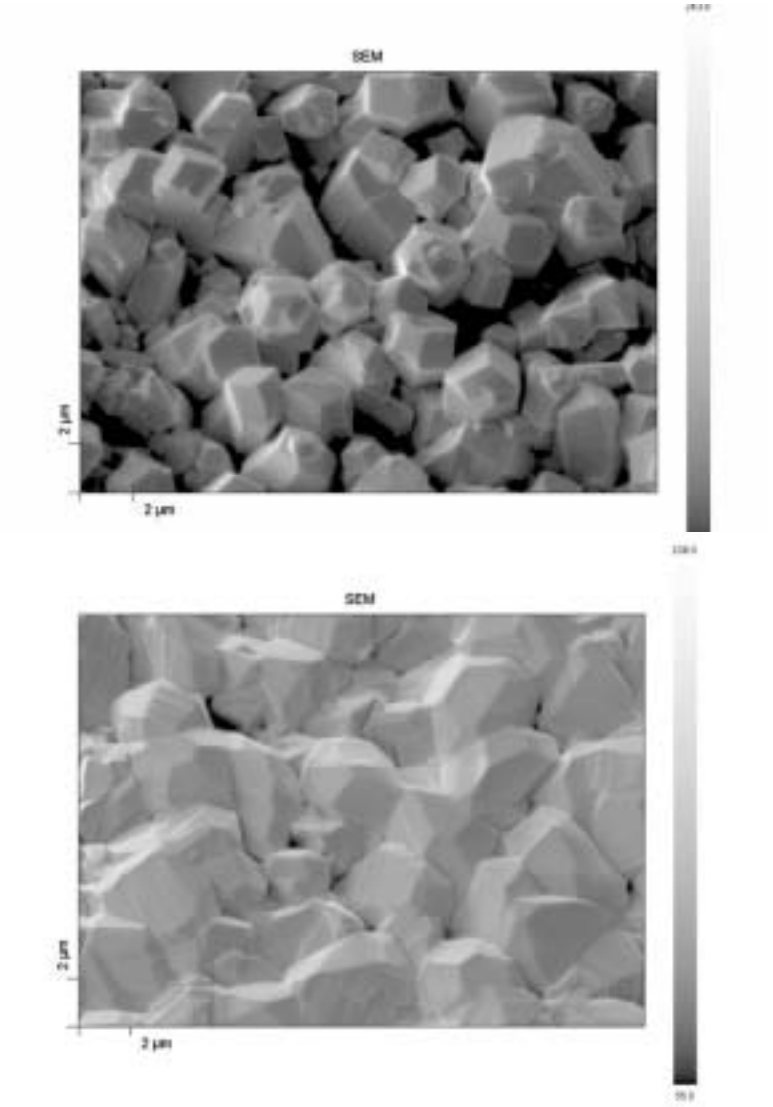

Figure 7. SEM images of CZT films deposited on CdS-top and SnO_2-bottom.

suggest that it is necessary to study this process in more detail and better understand what affects the nucleation of CZT films in order to further improve their structural and electronic properties.

Device Performance

As indicated in previous reports, the performance of CZT-based solar cells is significantly limited due to low J_{SC}'s. This is being primarily attributed to the poor electronic properties of CZT that result in inefficient carrier collection. Most of the emphasis to improve the properties of CZT films has to-date been placed on using various heat treatments. This was based on experience with CdTe where heat treatments significantly affect their performance. Although heat-treatments continue to be a major activity, during this quarter an attempt was made to modify the properties of CZT films by adding N_2 (a potential p-type dopant) during the sputtering process. Figure 8 shows the V_{OC} and J_{SC} of several CZT/CdS devices for which the CZT films were deposited under different N_2 partial pressures. The "filled" symbols/solid lines mark the V_{OC} and the "empty" symbols and dotted lines mark J_{SC}. Diamonds are for as-deposited devices and squares for heat-treated devices in inert ambient (He) at 500ºC. In all cases both quantities are significantly lower than their ideal levels. Although the actual amount of N incorporation in these CZT films is not yet known, apparently there exists an "optimum" level that can improve the performance of CZT-based devices. A post-deposition heat-treatment seems to further improve the overall performance but the increases are modest. The above results indicate that the electronic properties of CZT thin films can be varied to a certain extent. Nevertheless, they also point to the difficulties associated with CZT-based devices and the need to develop processing schemes that can yield films with improved electronic properties.

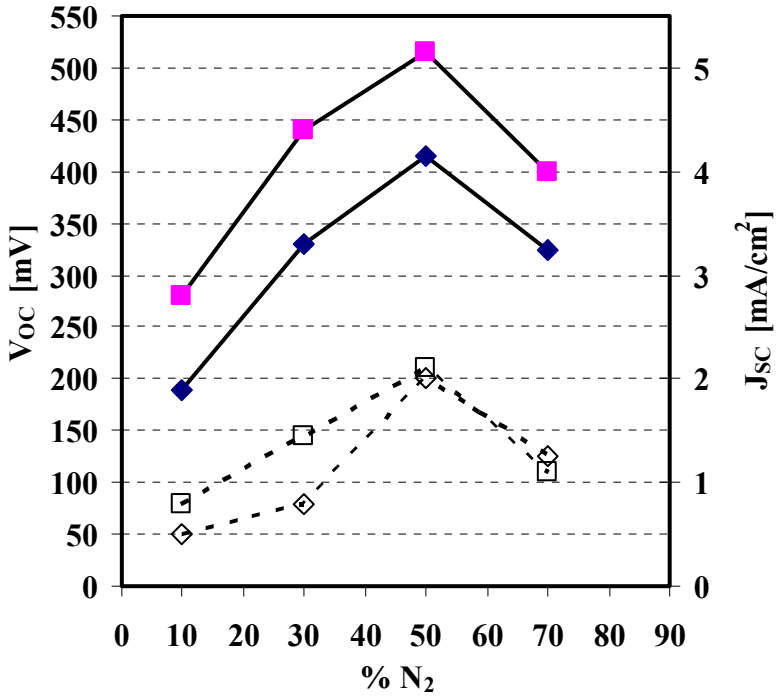

Figure 8 V_{OC} and FF of CST/CdS thin film solar cells as a function of the amount of N_2 used during the sputtering process.

SIMS Analysis

A series of CZT/window structures (CZT prepared by CSS) was recently evaluated at NREL[†]. Figure 9 shows two of the profiles: these are for ZnTe/CZT/CdS (left) and CZT/ZnSe (right) junctions. For the CZT/CdS junction the profiles for Zn, Cd and Te are

[†] We wish to thank Sally Asher and her group for these measurements.

essentially constant through the CZT layer, while for the CZT/ZnSe junction there appears to be a gradient for some of these elements, in particular Cd; at this time it is not clear whether these gradients are related to the deposition process or are measurements artifacts. The CZT/ZnSe junction interface appears to be better defined than the CZT/CdS interface, where some interdiffusion appears to have taken place between CZT and CdS (note that the Zn signal increases in the CdS region). These results clearly demonstrate the compositional uniformity attainable with the co-CSS process, as well as the need to further investigate the nature of the CZT/window interface where interdiffusion appears to be influenced by the window layer. Although, interdiffusion at the CdTe/CdS interface of CdTe-based solar cells is beneficial, its effect on CZT devices is not known at this time.

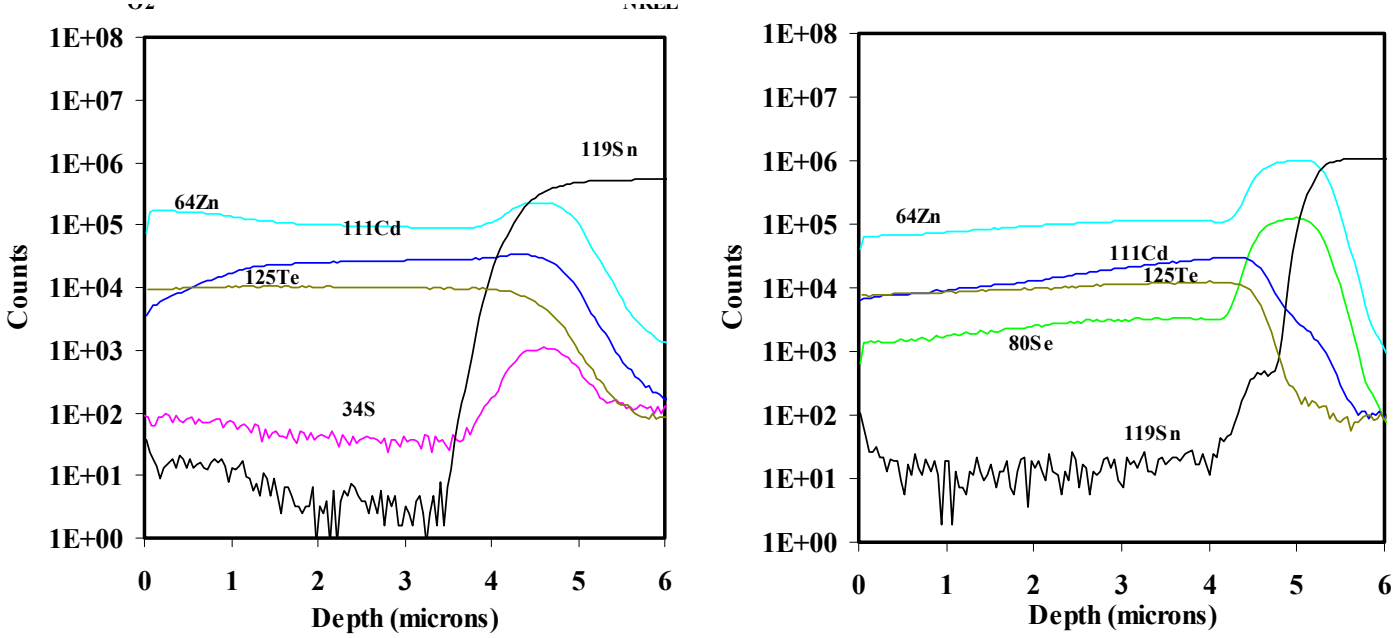

Figure 9 SIMS depth profiles for ZnTe/CZT/CdS (left) and CZT/ZnSe (right) structures.

Future Activities

Future work will continue to evaluate CZT devices fabricated by both CSS and sputtering. In the CSS area all devices will include ZnTe in order to "plug" the pinholes and eliminate shunts, and the most promising heat treatments previously utilized for structures without ZnTe will be revisited. The effect of the window layers on the properties of CZT will also be investigated in more detail. Work on constructing a new deposition apparatus where up to three films can be in-situ deposited by co-CSS is also underway. The system is an improved version of the currently utilized apparatus in an effort to improve spatial uniformity.

References

S. Zhang, S. Wei, and A. Zunger, *J. Appl. Phys.*, **83**(6), 3192 (1998).